What is claimed is:

1. A method for generating an optimized circuit that implements a program implemented in programmable logic, the method comprising:

analyzing a circuit implemented in the programmable logic for possible optimizations; and

optimizing the circuit into the optimized circuit to provide a more efficient implementation of the program by executing a portion of the program using software constructs, wherein using software constructs comprises establishing communications between the programmable logic circuit and at least one software device.

2. The method of claim 1 wherein analyzing the circuit comprises using a software-to-hardware compiler to analyze the circuit at a later stage in a compilation.

3. The method of claim 1 wherein analyzing the circuit comprises analyzing the circuit's critical path.

4. The method of claim 1 wherein optimizing the circuit comprises placing at least one register in the circuit.

5. The method of claim 1 wherein optimizing the circuit comprises placing at least one FIFO in the circuit.

6. The method of claim 1 wherein optimizing the circuit comprises placing at least one interface buffer in the circuit.

7. A communication interface between a first device and a second device, the interface comprising:

a communication channel between the first device and the second device;

at least one pop interface buffer that pops data on the first device, wherein the data is received from the communication channel;

at least one push interface buffer that places the data onto the communications channel from the second device, wherein each push interface buffer has a corresponding pop interface buffer across the communication channel, and wherein each pop interface buffer provides an acknowledgment to its corresponding push interface buffer.

8. The communication interface of claim 7 wherein the acknowledgment indicates that the corresponding pop interface buffer has popped an amount of data.

9. The communication interface of claim 7 wherein the communication channel is a bidirectional communication channel.

10. The communication interface of claim 7 further comprising:

a second communication channel, wherein:

the communication channel is unidirectional in a first direction, and

the second communication channel is unidirectional in a second direction, wherein the second direction is opposite the first direction;

at least one pop interface buffer that pops data on the second device, wherein the data is

received from the second communications channel;

at least one push interface buffer that places the data onto the second communications channel from the first device, wherein each push interface buffer has a corresponding pop interface buffer across the second communication channel, and wherein each pop interface buffer provides a second acknowledgment to its corresponding push interface buffer.

11. The communication interface of claim 10 wherein acknowledgments are communicated over the second communication channel.

12. The communication interface of claim 10 wherein second acknowledgments are communicated over the communication channel.

13. The communication interface of claim 7 wherein the communication channel comprises:

a channel multiplexer that combines data being sent from push interface buffers; and

a channel demultiplexer that determines to which pop interface buffers the data is to be forwarded.

14. The communication interface of claim 7 wherein the communication channel is based on a transport medium selected from a group consisting of a shared memory transport medium, a direct interconnect transport medium, and a bus-based transport medium.

15. The communication interface of claim 7 wherein the first device is selected from a group consisting of a hardware device and a software device.

16. The communication interface of claim 7 wherein the second device is selected from a group consisting of a hardware device and a software device.

17. A communication interface between a first device and a second device, the interface comprising:

a first unidirectional communication channel that carries data between the first device and the second device;

a second unidirectional communication channel that carries data between the first device and the second device in the opposite direction of the first unidirectional communication channel, wherein each of the first and second communication channels comprise:

a channel multiplexer that places data onto one of the communication channels, and

a channel demultiplexer that receives the data from the channel multiplexer and determines where to forward the data;

a first buffer that places an acknowledgment onto the channel multiplexer of the first unidirectional communication channel; and

a second buffer that receives the acknowledgment from the channel multiplexer of the second unidirectional communication channel.

18. The communication interface of claim 17 wherein the first buffer is a pop interface buffer and the second buffer is a push interface buffer.

19. The communication interface of claim 17 wherein the acknowledgment indicates that the first buffer is not full.

20. The communication interface of claim 17 wherein the first device is selected from a group consisting of a hardware device and a software device.

21. The communication interface of claim 17 wherein the second device is selected from a group consisting of a hardware device and a software device.

22. The communication interface of claim 17 wherein the first and second unidirectional communication channels are based on bus transport medium.